Attorney's Docket No. 042390P8995

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application for:	)	Examiner: Ngo, Chuong D.
Narsing K. Vijayrao, et al.	)	Art Unit: 2124
Serial No.: 09/604,620	)	Confirmation No.: 5234
Filed: June 27, 2000	)	
For: **METHOD AND APPARATUS FOR IMPROVING THE PERFORMANCE OF A FLOATING POINT MULTIPLIER ACCUMULATOR**	)	

APPEAL BRIEF

Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Applicants submit, in triplicate, the following Appeal Brief pursuant to 37 C.F.R. § 1.192 for consideration by the Board of Patent Appeals and Interferences. Applicants also submit herewith a check in the amount of $330.00 to cover the cost of filing the opening brief as required by 37 C.F.R. §1.17(c). Please charge any additional amount due or credit any overpayment to the Deposit Account 02-2666.

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I. REAL PARTY IN INTEREST

The real party in interest is Intel Corporation of Santa Clara, California.

II. RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences which will affect or be affected by the outcome of this appeal.

III. STATUS OF THE CLAIMS

Claims 1-23 are pending and rejected in this application.

IV. STATUS OF THE AMENDMENTS

Amendments to independent claims 1, 9, and 14 filed February 19, 2004, subsequent to the final rejection, have been entered but did not place the Application in condition for allowance.

V. SUMMARY OF INVENTION

According to embodiments of the invention, a floating point multiplier accumulator (FMAC) is provided having increased performance. (Abstract) For example, FMAC 300 receives as input floating point numbers A, B, and C. (page 5, lines 20-23; and **Figure 3**) Multiplier 304 of FMAC 300 receives A, B and C, produces A x B + C and outputs the result in SUM and CARRY form. (page 5, lines 23-24; and **Figure 3**) Propagate, kill, generate (PKG) generator 308 is coupled to multiplier 304 and receives the SUM and CARRY as input. (page 5, lines 24-25; and **Figure 3**) The PKG generator produces propagate (P), kill (K), and generate (G) using SUM and CARRY. (page 5, lines 26; and **Figure 3**)

Adder 310, plus-oner 312, plus-two-er 314, and leading zero anticipator 316 are coupled to PKG generator 308 and all receive P, K, and G as input. (page 5, lines 27-29; and **Figure 3**) Simultaneously, adder 310 uses P, K and G to add SUM and CARRY; plus-oner 312 uses P, K and G to add SUM and CARRY and increment the resulting sum by one; plus-two-er 314 uses P, K and G to add SUM and CARRY and increment the resulting sum by two; and leading zero anticipator (LZA) 316 determines the location of the decimal point of the result by computing a leading zero position. (Abstract; page 5, line 29 - page 6, line 2; and **Figure 3**) Multiplexor 320 receives the result of each of adder

310, plus-oner 312, and plus-two-er 314 and selects which of the results is appropriate responsive to a control signal received from rounding control 322 and the decimal point position from LZA. (Abstract; page 6, lines 2-5; and **Figure 3**)

A normalization shifter is coupled to the multiplexor and the LZA 316. (Abstract, **Figure 3**) Normalization shifter 326 receives as input the appropriate sum selected by multiplexor 320 and normalizes the selected appropriate sum, based on the decimal point position from LZA 316. (Abstract; page 6, lines 8-9; and **Figure 3**)

VI. ISSUES

The issues involved in this appeal are whether claims 1-23 are unpatentable under 35 U.S.C. § 103(a) as being obvious from Applicants' admission of prior art disclosed in **Figure 1** of the instant application (herein "APA") in view of Quach, et al. "An Improved Algorithm for High-Speed Floating-Point Addition" (herein "Quach").

VII. GROUPING OF THE CLAIMS

Applicant submits that the claims do not stand or fall together. Applicant groups the claims as follows:

Group I	: Claims 1-3, 6-10, and 12-13
Group II	: Claims 4-5
Group III	: Claim 11
Group IV	: Claims 14-16
Group V	: Claims 17-23

Applicant will argue why each of these groups of claims should be allowed below.

VIII. ARGUMENT

The Patent Office has rejected claims 1-23 under 35 U.S.C. § 103(a) as being obvious from APA in view of Quach.

A. Overview of the Invention and Cited References

1) Distinctive Features of the Invention

The distinctive features of the invention include: (1) a normalization shifter coupled to an output of the multiplexor and the LZA; (2) the PKG generator computes a propagate value (P), a kill value (K) and a generate value (G) based on the sum value

and the carry value; in parallel the adder adds the sum value and the carry value using P, K, and G; the plus-oner adds the sum value and the carry value using P, K, and G and increments by one; the plus-two-er adds the sum value and the carry value using P, K, and G and increments by two; (3) a propagate, kill, generate generator (PKG generator) to produce a propagate value (P), a kill value (K) and a generate value (G) coupled to the multiplier; in parallel the adder adds the sum value and the carry value using P, K, and G; the plus-oner adds the sum value and the carry value using P, K, and G and increments by one; and the plus-two-er adds the sum value and the carry value using P, K, and G and increments by two; (4) a second means for adding the sum value to the carry value and incrementing by one; a third means for adding the sum value to the carry value and incrementing by two; a means for determining a leading zero position, such that the first means for adding, the second means for adding, the third means for adding, and the means for determining are coupled in parallel to the means for computing (5) the means for selecting outputting a result from one of the first means for adding, the second means for adding, and the third means for adding responsive to the means for controlling; a means for normalizing coupled to an output of the means for selecting and the means for determining; (6) simultaneously ... adding the sum value to the carry value and incrementing by one to create a second result, adding the sum value to the carry value and incrementing by two to create a third result; (7) selecting one of the first result, the second result and the third result responsive to a rounding mode and the decimal point position as a selected result; normalizing the selected result based on the decimal point position.

2) Overview of the Cited Reference

APA

APA teaches reducing the steps and clock cycles necessary to perform a floating-point multiplication by combining and/or removing steps (see page 2, lines 19-24 and page 5, lines 14-19 of Applicant's specification) Specifically, APA teaches floating point multiplier accumulator (FMAC) 100 receiving floating point numbers A, B, and C as input and output a properly rounded result of "(A x B + C)" based on the rounding mode. (page 4, lines 5-7; and **Figure 1**) Specifically, FMAC 100 includes multiplier 102 to receive A, B, and C and output what is known as SUM and CARRY. (page 4, lines 7-8;

and **Figure 1**) Propagate, kill, generate (PKG) generator 104 is coupled to multiplier 102; receives SUM and CARRY; and using SUM and CARRY produces (1) P, the product of A and B, (2) G, the sum of A and B, and (3) K, the product of the one's complement of A and the one's complement of B. (page 4, lines 8-15; and **Figure 1**)

Adder 106 is coupled to the PKG generator and receives as input P, K and G and uses P, K and G to determine the sum of SUM and CARRY. (page 4, lines 16-17; and **Figure 1**) Leading zero anticipator (LZA) 108 is also coupled to the PKG generator and receives P, K and G from the PKG generator. (page 4, lines 18-19; and **Figure 1**) Normalization shifter 110 receives as input the result from adder 106 and the position of the decimal point from leading zero anticipator 108. (page 4, lines 19-21; and **Figure 1**) Rounding unit 112 receives the normalized result from normalization shifter 110, and then increments, decrements or leaves unaffected the normalized result, depending on the rounding mode. (page 4, lines 21-2; and **Figure 1**) In one prior art embodiment, rounding in the form of incrementing or decrementing requires at least one clock cycle. (page 4, lines 29-30; and **Figure 1**) In this prior art implementation, the total time for the FMAC processing includes the time needed to sequentially perform SUM plus CARRY addition and in adder 106 then perform rounding in rounding unit 112, if needed. (page 4, line 30 - page 5, line 2; and **Figure 1**)

Quach

Quach teaches reducing the steps and clock cycles necessary to perform a floating-point addition algorithm by combining and/or removing steps required by calculating variable "Cin" based on a mathematical theory of a floating-point addition where Cin selects results of a "g" path or a "l" path. (page 3) Specifically, Quach teaches an algorithm where normalizing is either required prior to selection of the "g" path or the "l" path (Table 2 "d ≤ 1 and Effective Subtraction" column), or where normalizing is not preformed at all because it is mutually exclusive with other floating-point addition algorithm processes along the alignment path taken (page 2 section "3", page 3 second and third paragraphs, and Tables 1 and 2 "Others" column). Moreover particularly, Quach teaches floating point addition process that assumes the significants of the 2 inputs (A, B) are already normalized and with that assumption, then shows that (A+B), (A+B+1) and (A+B+2) are sufficient to provide results that may be selected to

provide for floating point addition of two numbers. (tables 2 and 3; pages 2-4, and 15-16)

For example, according to the floating-point addition algorithm processes taught by Quach, in the IEEE round to nearest (RTN) mode, computing A+B and A+B+1 is sufficient to account for all the normalization possibilities, so that, by selecting the results using Cin computed based on the lower order bits of the significands, complementation and rounding can be done simultaneously, saving one addition step. (page 3, lines 7-10) Consequently, according to the teachings of Quach, either normalization is not required in this example, or occurs prior to the "select" step of the process for selecting A+B or A+B+1 according to Cin. (Tables 2 and 3, page 2 section "3", and page 3 second and third paragraphs).

B. Errors of Law and Fact

1) Specific limitations of Group I not obvious from the cited references.

Claims 1-3, 6-10, and 12-13 require (as claims 2-3, 6-8 depend from claim 1, and claims 10 and 12-13 depend from claim 9) a normalization shifter coupled to an output of the multiplexor and the LZA.

2) Explanation why such limitations render Group I unobvious by the cited references.

First, Claims 1-3, 6-10, and 12-13 are patentable over the cited references for at least the reason that the cited references do not teach "a normalization shifter coupled to an output of the multiplexor and the LZA," as required by claims 1-3, 6-10, and 12-13. To render a claim obvious, all elements of the claim must be taught or suggested by at least one properly combined reference of the combination.

In the Patent Office's rejection of claims 1-3, 6-10, and 12-13, the Patent Office cites normalization shifter 110 of the APA coupled to an output of the multiplexer of Quach in order to normalize the selected rounded output from the multiplexer. (Final Office Action mailed 11/19/03, page 2; and Advisory Action mailed 3/10/04, continuation page) However, normalization shifter 110 of the

APA combined with Quach does not teach or suggest the above quoted limitation of claims 1-3, 6-10, and 12-13 for at least four reasons.

The APA teaches normalization shifter 110 coupled to an output of adder 106 and to an input of rounding unit 112. (see Figure 1 and page 4, lines 19-21 of Applicant's specification). According to the APA, rounding unit 112 receives the normalized result from normalization shifter 110, and then increments, decrements or leaves unaffected the normalized result, depending on the rounding mode. (page 4, lines 21-2; and **Figure 1**) In addition, the APA does not teach or suggest a multiplexer for selecting outputs of one or more adders, but instead teaches rounding in the form of incrementing or decrementing requires at least one clock cycle. (page 4, lines 29-30; and **Figure 1**) Thus, according to the APA, the total time for the FMAC processing includes the time needed to sequentially perform SUM plus CARRY addition and in adder 106 then perform rounding in rounding unit 112, if needed. (page 4, line 30 - page 5, line 2; and **Figure 1**) Consequently, the Patent Office has not identified and Applicants are unable to find any teaching in the APA of a normalization shifter coupled to an output of a multiplexor, as required by claims 1-3, 6-10, and 12-13.

Moreover, Quach teaches reducing the steps and clock cycles necessary to perform a floating-point addition algorithm by combining and/or removing steps required by calculating Cin based on a mathematical theory of a floating-point addition where Cin selects results of the "g" path or the "l" path (see Quach, page 3). Specifically, Quach teaches an algorithm where normalizing is either required prior to selection of the "g" path or the "l" path (see Quach Table 2 "d $\leq$ 1 and Effective Subtraction" column), or where normalizing is not preformed at all because it is mutually exclusive with other floating-point addition algorithm processes along the alignment path taken (page 2 section "3", page 3 second and third paragraphs, and Tables 1 and 2 "Others" column).

Moreover particularly, Quach's teaches floating point addition process that assumes the significants of the 2 inputs (A, B) are already normalized and with that assumption, then shows that (A+B), (A+B+1) and (A+B+2) are sufficient to provide

results that may be selected to provide for floating point addition of two numbers. (tables 2 and 3; pages 2-4, and 15-16) For example, at page 3, lines 7-10, Quach states:

> In the IEEE *round to nearest* (*RTN*) mode, computing *A*+*B* and *A*+*B*+1 is sufficient to account for all the normalization possibilities to be discussed below. By selecting the results using C_{in} computed based on the lower order bits of the significands, complementation and rounding can be done simultaneously, saving one addition step. [emphasis added]

Consequently, according to this example, either normalization is not required, or occurs prior to the multiplexer selecting A+B or A+B+1 according to Cin. (Tables 2 and 3, page 2 section "3", and page 3 second and third paragraphs). Therefore, Quach teaches normalization prior to the "select" step (see Quach Tables 2 and 3, page 2 section "3", and page 3 second and third paragraphs). On the other hand, the Patent Office has not identified and Applicants are unable to find any teaching or suggestion in Quach of a normalization shifter coupled to an output of the multiplexor, as required by claims 1-3, 6-10, and 12-13.

Hence, for at least the first reason that neither the APA, Quach, nor the combination teach the above quoted limitations of claims 1-3, 6-10, and 12-13, Applicants requests that the Board overturn the rejection of claims 1-3, 6-10, and 12-13 as being unpatentable over the APA and Quach under 35 U.S.C. §103(a).

Second, Applicants submit that the APA can not be properly combined with Quach because the combination would render the APA as well as Quach unsatisfactory for their intended purposes. The combination would render Quach unsatisfactory for its intended purposes of reducing the steps and clock cycles necessary to perform a floating-point addition algorithm by combining and/or removing steps (see Quach, page 3). Similarly, the combination would render the APA unsatisfactory for its intended purposes of reducing the steps and clock cycles necessary to perform a floating-point multiplication by combining and/or removing steps (see page 2, lines 19-24 and page 5, lines 14-19 of Applicant's specification) Applicants point out that the Patent Office verifies these intended purposes by specifying that the motive for combining the APA with Quach is "in order to perform … with a reduced processing stages, and thus to reduce the processing time." (Final Office Action mailed 11/19/03, page 3)

First, Quach's floating-point addition algorithm to calculate variable "Cin" based on a mathematical theory of a floating-point addition to select results of a "g" path or a "l" path can not be combined with the APA as suggested by the Patent Office without requiring additional algorithm steps. Notably, Quach 's teachings are not able to handle the floating point multiplication and accumulation (FMAC) of the APA without additional steps because Quach's floating point addition teachings assume the significants of the 2 inputs (A, B) are already normalized. Then with that assumption, Quach 's teachings show that (A+B), (A+B+1) and (A+B+2) are sufficient to provide results that may be selected to provide for floating point addition of two numbers. (tables 2 and 3; pages 2-4, and 15-16) On the other hand, according to teachings of the FMAC application of the APA, A*B+C, A*B may yield a result greater than or equal to 2 (e.g., such as, 1.1 * 1.1 = 10.01), which is not normalized after being selected. (page 5, lines 23-29; and **Figure 3**)

For example, according to the floating-point addition algorithm processes taught by Quach for IEEE *round to nearest* (*RTN*) mode, where computing *A+B* and *A+B*+1 is sufficient to account for all the normalization possibilities, selecting the results of *A+B* and *A+B*+1 using Cin computed based on the lower order bits of the significands allows for complementation and rounding to be done simultaneously, saving one addition step. (page 3, lines 7-10) However, if normalization is required, it occurs prior to the "select" step of the process for selecting A+B or A+B+1 according to Cin. (Tables 2 and 3, page 2 section "3", and page 3 second and third paragraphs).

Thus, combining Quach with the APA to teach the limitations of claims 1-3, 6-10, and 12-13 quoted above, would at least require one normalization step after the adders and before the multiplexer (e.g., as required for the mathematical teachings of Quach to apply, such as those related to Table 2) and a second normalization step after the multiplexer to read on the limitations of claims 1-3, 6-10, and 12-13. In other words, combining the APA with Quach would require additional steps to normalize the multiple of A*B output of the adders, prior to selection by the multiplexer (e.g., such as is shown in Table 2 of Quach). Therefore, use of two normalization steps would render Quach and the APA unsatisfactory for their intended purposes of combining steps, reducing steps, and reducing clock cycles necessary to perform a floating-point addition and multiplication algorithms. (see MPEP §2143.01 and MPEP Section 2145.X.D).

Furthermore, in Quach's work, d = | Ea - Eb | and one of the significands needs to be 2's complemented. However, to combine the APA FMAC application and Quach's approach to FMAC applications, additional steps would be required to make the product of A*B in 2's complemented form. Thus, the added steps to make the product of A*B in 2's complemented form would render Quach and the APA unsatisfactory for their intended purposes of combining steps, reducing steps, and reducing clock cycles necessary to perform a floating-point addition and multiplication algorithms (see MPEP §2143.01 and MPEP Section 2145.X.D).

Hence, for at least the second reason that combining the APA with Quach would render the APA unsatisfactory for its intended purpose, and the third reasons that combining the APA with Quach would render Quach unsatisfactory its intended purpose, Applicants requests that the Board overturn the rejection of claims 1-3, 6-10, and 12-13 as being unpatentable over the APA and Quach under 35 U.S.C. §103(a).

Next, since neither reference provides a motive to combine and since combining the references would render APA and Quach unsatisfactory for either of their intended purposes, Applicants can only conclude that the motive to combine the references includes knowledge gleaned only from Applicants' disclosure, hence Applicants assert that the combination of APA with Quach is the result of impermissible hindsight in accordance with MPEP § 2144.X.D.

Thus, for at least the fourth reason that the combination of APA with Quach is the result of impermissible hindsight, Applicants requests that the Board overturn the rejection of claims 1-3, 6-10, and 12-13 as being unpatentable over the APA and Quach under 35 U.S.C. §103(a).

3) Specific limitations of Group II not obvious from the cited references.

Throughout the following argument, it is assumed that the dependent claims carry with them the arguments made in favor of base claims and any intervening claims.

Claims 4-5 further require (as claim 5 depends from claim 4, and claim 4 depends from claims 1-3) that the PKG generator computes a propagate value (P), a kill value

(K) and a generate value (G) based on the sum value and the carry value; and in parallel the adder adds the sum value and the carry value using P, K, and G; the plus-oner adds the sum value and the carry value using P, K, and G and increments by one; and the plus-two-er adds the sum value and the carry value using P, K, and G and increments by two.

4) Explanation why such limitations render Group II unobvious by the cited references.

Applicant submits that dependent claims 4-5 are further patentable over the cited references for at least the reason that those references do not teach or suggest that the PKG generator computes a propagate value (P), a kill value (K) and a generate value (G) based on the sum value and the carry value; and in parallel the adder adds the sum value and the carry value using P, K, and G; the plus-oner adds the sum value and the carry value using P, K, and G and increments by one; and the plus-two-er adds the sum value and the carry value using P, K, and G and increments by two, as required by dependent claims 4-5. To render a claim obvious, all elements of the claim must be taught or suggested by at least one properly combined reference of the combination.

The Patent Office relies upon the APA and Quach page 3, lines 4-10 and footnote 1 to teach the limitations cited above. (Final Office Action mailed 11/19/03, page 2) The APA teaches addition of P, K, and G to determine the sum of SUM and CARRY. (page 4, lines 7-17; and **Figure 1**) However, the APA does not teach adding the SUM value and the CARRY value and incrementing by 1, nor adding the SUM value and the CARRY value and incrementing by 2, as required by the limitations of claims 4-5 cited above. Moreover, Quach teaches adding significants of a first number "A" and a second number "B", adding A+B and incrementing by 1, and adding A+B and incrementing by 2. (tables 2 and 3; pages 2-4, and 15-16)

However, the Patent Office has not identified and Applicants are unable to find any suggestion or teaching in the APA or Quach that accounts for in parallel ... the plus-oner adds the sum value and the carry value using P, K, and G and increments by one; and the plus-two-er adds the sum value and the carry value using P, K, and G and increments by two. Therefore, since neither APA, Quach, nor the combination thereof teaches or suggests the limitation of claims 4-5 cited above, Applicants request that the

Board overturn the rejection of dependent claims 4-5 as being anticipated for at least this further reason.

5) **Specific limitation of Group III not obvious from the cited references.**

Throughout the following argument, it is assumed that the dependent claims carry with them the arguments made in favor of base claims and any intervening claims.

Claim 11 further requires (as claims 11 depends from claims 9-10) that a propagate, kill, generate generator (PKG generator) to produce a propagate value (P), a kill value (K) and a generate value (G) coupled to the multiplier; and in parallel the adder adds the sum value and the carry value using P, K, and G; the plus-oner adds the sum value and the carry value using P, K, and G and increments by one; and the plus-two-er adds the sum value and the carry value using P, K, and G and increments by two.

6) **Explanation why such limitations render Group III unobvious by the cited references.**

Applicant submits that dependent claim 11 is further patentable over the cited references for at least the reason that those references do not teach or suggest a propagate, kill, generate generator (PKG generator) to produce a propagate value (P), a kill value (K) and a generate value (G) coupled to the multiplier; and in parallel the adder adds the sum value and the carry value using P, K, and G; the plus-oner adds the sum value and the carry value using P, K, and G and increments by one; and the plus-two-er adds the sum value and the carry value using P, K, and G and increments by two, as required by dependent claim 11. To render a claim obvious, all elements of the claim must be taught or suggested by at least one properly combined reference of the combination.

The Patent Office relies upon the APA and Quach page 3, lines 4-10 and footnote 1 to teach the limitations cited above. (Final Office Action mailed 11/19/03, page 2) As a result, an argument analogous to the one above with respect to claims 4-5, also applies here.

Correspondingly, the Patent Office has not identified and Applicants are unable to find any suggestion or teaching in the APA or Quach that accounts for in parallel … the plus-oner adds the sum value and the carry value using P, K, and G and increments by one; and the plus-two-er adds the sum value and the carry value using P, K, and G and increments by two. Therefore, since neither APA, Quach, nor the combination thereof teaches or suggests the limitation of claim 11 cited above, Applicants request that the Board overturn the rejection of dependent claim 11 as being anticipated for at least this further reason.

7) Specific limitations of Group IV not obvious from the cited references.

Claims 14-16 require (as claims 15-16 depend from claim 14): (1) a second means for adding the sum value to the carry value and incrementing by one; a third means for adding the sum value to the carry value and incrementing by two; a means for determining a leading zero position, such that the first means for adding, the second means for adding, the third means for adding, and the means for determining are coupled in parallel to the means for computing; and (2) the means for selecting outputting a result from one of the first means for adding, the second means for adding, and the third means for adding responsive to the means for controlling; a means for normalizing coupled to an output of the means for selecting and the means for determining.

8) Explanation why such limitations render Group IV unobvious by the cited references.

First, Claims 14-16 are patentable over the cited references for at least the reason that the cited references do not teach "a second means for adding the sum value to the carry value and incrementing by one; a third means for adding the sum value to the carry value and incrementing by two; … the second means for adding, the third means for adding, … are coupled in parallel …," as required by claims 14-16. To render a claim obvious, all elements of the claim must be taught or suggested by at least one properly combined reference of the combination.

The Patent Office relies upon the APA and Quach page 3, lines 4-10 and footnote 1 to teach the limitations cited above. (Final Office Action mailed 11/19/03, page 2) As a

result, an argument analogous to the one above with respect to claims 4-5, also applies here.

Correspondingly, the Patent Office has not identified and Applicants are unable to find any suggestion or teaching in the APA or Quach that accounts for a second means for adding the sum value to the carry value and incrementing by one; and a third means for adding the sum value to the carry value and incrementing by two; where the second and third means for adding are coupled in parallel. Therefore, since neither APA, Quach, nor the combination thereof teaches or suggests the limitation of claims 14-16 cited above, Applicants request that the Board overturn the rejection of claims 14-16 as being anticipated for at least this first reason.

Second, Claims 14-16 are patentable over the cited references for at least the reason that the cited references do not teach "the means for selecting outputting a result from one of the first means for adding, the second means for adding, and the third means for adding responsive to the means for controlling; a means for normalizing coupled to an output of the means for selecting and the means for determining," as required by claims 14-16.

The Patent Office relies upon normalization shifter 110 of the APA coupled to an output of the multiplexer of Quach in order to normalize the selected rounded output from the multiplexer. (Final Office Action mailed 11/19/03, page 2; and Advisory Action mailed 3/10/04, continuation page) As a result, an argument analogous to the one above with respect to claims 1-3, 6-10, and 12-13, also applies here.

Correspondingly, the Patent Office has not identified and Applicants are unable to find any suggestion or teaching in the APA or Quach that accounts for a means for normalizing coupled to an output of the means for selecting a result from one of the first means for adding, the second means for adding, and the third means for adding. Therefore, since neither APA, Quach, nor the combination thereof teaches or suggests the limitation of claims 14-16 cited above, Applicants request that the Board overturn the rejection of claims 14-16 as being anticipated for at least this second reason.

Furthermore, Applicants assert that Claims 14-16 are patentable over the cited references for at least the third and fourth reasons that combining the APA with Quach would render the APA and Quach unsatisfactory for their intended purposes as described above with respect to claims 1-3, 6-10, and 12-13. Thus, Applicants requests that the Board overturn the rejection of claims 14-16 as being unpatentable over the APA and Quach under 35 U.S.C. §103(a) for at least these two additional reasons.

Next, for at least the fourth reason that the combination of APA with Quach is the result of impermissible hindsight as described above with respect to claims 1-3, 6-10, and 12-13, Applicants requests that the Board overturn the rejection of claims 14-16 as being unpatentable over the APA and Quach under 35 U.S.C. §103(a).

9) Specific limitations of Group V not obvious from the cited references.

Claims 17-23 require (as claims 18-19 depend from claim 17, and claims 22-23 depend from claim 21): (1) simultaneously ... adding the sum value to the carry value and incrementing by one to create a second result, adding the sum value to the carry value and incrementing by two to create a third result; and (2) selecting one of the first result, the second result and the third result responsive to a rounding mode and the decimal point position as a selected result; and normalizing the selected result based on the decimal point position.

10) Explanation why such limitations render Group V unobvious in view of the cited references.

First, Claims 17-23 are patentable over the cited references for at least the reason that the cited references do not teach "simultaneously ... adding the sum value to the carry value and incrementing by one to create a second result, adding the sum value to the carry value and incrementing by two to create a third result," as required by claims 17-23. To render a claim obvious, all elements of the claim must be taught or suggested by at least one properly combined reference of the combination.

The Patent Office relies upon the APA and Quach page 3, lines 4-10 and footnote 1 to teach the limitations cited above. (Final Office Action mailed 11/19/03, page 2) As a

result, an argument analogous to the one above with respect to claims 4-5, also applies here.

Correspondingly, the Patent Office has not identified and Applicants are unable to find any suggestion or teaching in the APA or Quach that accounts for simultaneously adding the sum value to the carry value and incrementing by one, and adding the sum value to the carry value and incrementing by two. Therefore, since neither APA, Quach, nor the combination thereof teaches or suggests the limitation of claims 17-23 cited above, Applicants request that the Board overturn the rejection of claims 17-23 as being anticipated for at least this first reason.

Second, Claims 17-23 are patentable over the cited references for at least the reason that the cited references do not teach "selecting one of the first result, the second result and the third result responsive to a rounding mode and the decimal point position as a selected result; and normalizing the selected result based on the decimal point position," as required by claims 17-23.

The Patent Office relies upon normalization shifter 110 of the APA coupled to an output of the multiplexer of Quach to normalize the selected rounded output from the multiplexer. (Final Office Action mailed 11/19/03, page 2; and Advisory Action mailed 3/10/04, continuation page) As a result, an argument analogous to the one above with respect to claims 1-3, 6-10, and 12-13, also applies here.

Correspondingly, the Patent Office has not identified and Applicants are unable to find any suggestion or teaching in the APA or Quach that accounts for normalizing the selected result of the sum of the sum value added to the carry value, the sum value added to the carry value and incremented by one, and the sum value added to the carry value and incremented by two. Therefore, since neither APA, Quach, nor the combination thereof teaches or suggests the limitation of claims 17-23 cited above, Applicants request that the Board overturn the rejection of claims 17-23 as being anticipated for at least this second reason.

Furthermore, Applicants assert that Claims 17-23 are patentable over the cited references for at least the third and fourth reasons that combining the APA

limitation of claims 17-23 cited above, Applicants request that the Board overturn the rejection of claims 17-23 as being anticipated for at least this second reason.

Furthermore, Applicants assert that Claims 17-23 are patentable over the cited references for at least the third and fourth reasons that combining the APA with Quach would render the APA and Quach unsatisfactory for their intended purposes as described above with respect to claims 1-3, 6-10, and 12-13. Thus, Applicants requests that the Board overturn the rejection of claims 17-23 as being unpatentable over the APA and Quach under 35 U.S.C. §103(a) for at least these two additional reasons.

Next, for at least the fourth reason that the combination of APA with Quach is the result of impermissible hindsight as described above with respect to claims 1-3, 6-10, and 12-13, Applicants requests that the Board overturn the rejection of claims 17-23 as being unpatentable over the APA and Quach under 35 U.S.C. §103(a).

IX. CONCLUSION AND RELIEF

Based on the foregoing, Applicant requests that the Board overturn the Examiner's rejection of all pending claims and hold that all of the claims of the present application are allowable.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to: Mail Stop Appeal Brief – Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on June 4, 2004.

Jean Svoboda

X. APPENDIX A

1. (Previously Presented) A significand portion of a floating point multiply accumulator (FMAC) comprising:

a multiplier receiving a first input significand, a second input significand, and a third input significand;

a propagate, kill, generate generator (PKG generator) coupled to the multiplier;

an adder, a plus-oner, a plus-two-er and a leading zero anticipator (LZA) each coupled to the PKG generator;

a rounding control unit coupled to the LZA;

a multiplexor coupled to each of the adder, the plus-oner, the plus-two-er and the rounding control unit; and

and a normalization shifter coupled to an output of the multiplexor and the LZA.

2. (Original) The significand portion of Claim 1 wherein the multiplier outputs a sum value and a carry value.

3. (Original) The significand portion of Claim 2 wherein the PKG generator computes a propagate value (P), a kill value (K) and a generate value (G) based on the sum value and the carry value.

4. (Original) The significand portion of Claim 3 wherein in parallel the adder adds the sum value and the carry value using P, K, and G; the plus-oner adds the sum value and the carry value using P, K, and G and increments by one; and the plus-two-er adds the sum value and the carry value using P, K, and G and increments by two.

5. (Original) The significand portion of Claim 4 wherein the LZA computes in parallel with the adder, the plus-oner, and the plus-two-er.

6. (Original) The significand portion of Claim 1 wherein the rounding control unit reads a rounding mode from a register in a processor in which the FMAC resides.

7. (Original) The significand portion of Claim 1 wherein the normalization shifter and the rounding control unit each receive a leading zero position indication from the LZA.

8. (Original) The significand portion of Claim 1 wherein the multiplexor produces an output result responsive to the rounding control unit.

9. (Previously Presented) A floating point multiply accumulator (FMAC) comprising:

a multiplier;

a propagate, kill, generate generator (PKG generator) to produce a propagate value (P), a kill value (K) and a generate value (G) coupled to the multiplier;

an adder, a plus-oner, a plus-two-er and a leading zero anticipator (LZA) each coupled to the PKG generator in parallel;

a rounding control unit coupled to the LZA and coupled to a multiplexor, the multiplexor outputting a result from one of the adder, the plus-oner, and the plus-two-er responsive to the rounding control unit; and

and a normalization shifter coupled to an output of_the multiplexor and the LZA.

10. (Original) The FMAC of Claim 9 wherein the multiplier produces a product of a first floating point number and a second floating point number added to a third floating point number as a sum value and a carry value.

11. (Original) The FMAC of Claim 10 wherein in parallel the adder adds the sum value and the carry value using P, K, and G; the plus-oner adds the sum value and the carry value using P, K, and G and increments by one; and the plus-two-er adds the sum value and the carry value using P, K, and G and increments by two.

12. (Original) The FMAC of Claim 9 wherein the rounding control unit outputs a select signal to the multiplexor based on a rounding mode and the decimal point position.

13. (Original) The FMAC of Claim 9 wherein the normalization shifter normalizes based on the decimal point position.

14. (Previously Presented) A floating point multiply accumulator (FMAC) comprising:

a means for multiplying a first significand and a second significand and adding a third significand to produce a sum value and a carry value;

a means for computing a propagate value, a kill value, and a generate value coupled to the means for multiplying;

a first means for adding the sum value to the carry value;

a second means for adding the sum value to the carry value and incrementing by one;

a third means for adding the sum value to the carry value and incrementing by two;

a means for determining a leading zero position, such that the first means for adding, the second means for adding, the third means for adding, and the means for determining are coupled in parallel to the means for computing;

a means for controlling responsive to the means for determining and a rounding mode, the means for controlling further coupled to a means for selecting, the means for selecting outputting a result from one of the first means for adding, the second means for adding, and the third means for adding responsive to the means for controlling; and

a means for normalizing coupled to an output of the means for selecting and the means for determining.

15. (Original) The FMAC of Claim 14 wherein the means for controlling reads the rounding mode from a register in a processor in which the FMAC resides.

16. (Original) The FMAC of Claim 14 wherein the means for normalizing is responsive to the means for determining.

17. (Original) A method in a floating point multiply accumulator (FMAC) comprising:

receiving a first floating point number, a second floating point number and a third floating point number;

computing a product of the first floating point number and the second floating point number and adding a third floating point number to produce a sum value and a carry value;

computing a propagate value, a kill value and a generate value based on the sum value and the carry value;

simultaneously adding the sum value to the carry value to create a first result, adding the sum value to the carry value and incrementing by one to create a second result, adding the sum value to the carry value and incrementing by two to create a third result, and determining a decimal point position;

selecting one of the first result, the second result and the third result responsive to a rounding mode and the decimal point position as a selected result; and

normalizing the selected result based on the decimal point position.

18. (Original) The method of Claim 17 further comprising;

reading the rounding mode from a register in a processor in which the FMAC resides.

19. (Original) The method of Claim 17 wherein normalizing comprises:
shifting the bits in the selected result.

20. (Original) The method of Claim 17 wherein the propagate value, the kill value and the generate value are used by the adder, the plus-oner and the plus-two-er to compute the first result, the second result and the third result.

21. (Original) A machine readable medium containing instructions which, when executed by a processor, cause a machine to perform operations comprising:

receiving a first floating point number, a second floating point number and a third floating point number;

computing a product of the first floating point number and the second floating point number and adding a third floating point number to produce a sum value and a carry value;

computing a propagate value, a kill value and a generate value based on the sum value and the carry value;

simultaneously adding the sum value to the carry value to create a first result, adding the sum value to the carry value and incrementing by one to create a second result, adding the sum value to the carry value and incrementing by two to create a third result, and determining a decimal point position;

selecting one of the first result, the second result and the third result responsive to a rounding mode and the decimal point position as a selected result; and

normalizing the selected result based on the decimal point position.

22. (Original) The machine readable medium of Claim 21 containing instructions which, when executed by a processor, cause the machine to perform further operations comprising:

reading the rounding mode from a register in a processor in which the FMAC resides.

23. (Original) The machine readable medium of Claim 21 wherein normalizing comprises:

shifting the bits in the selected result.